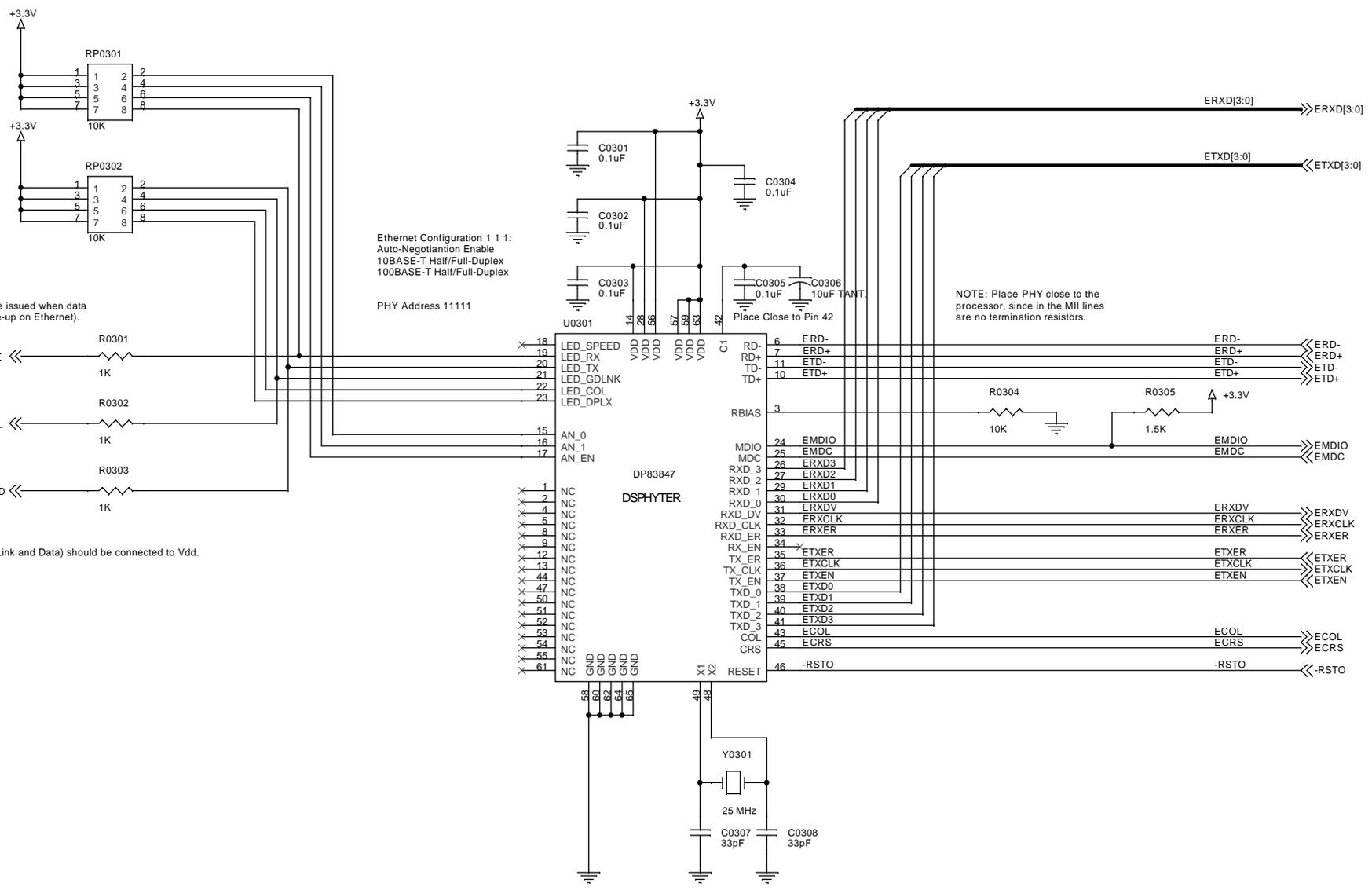


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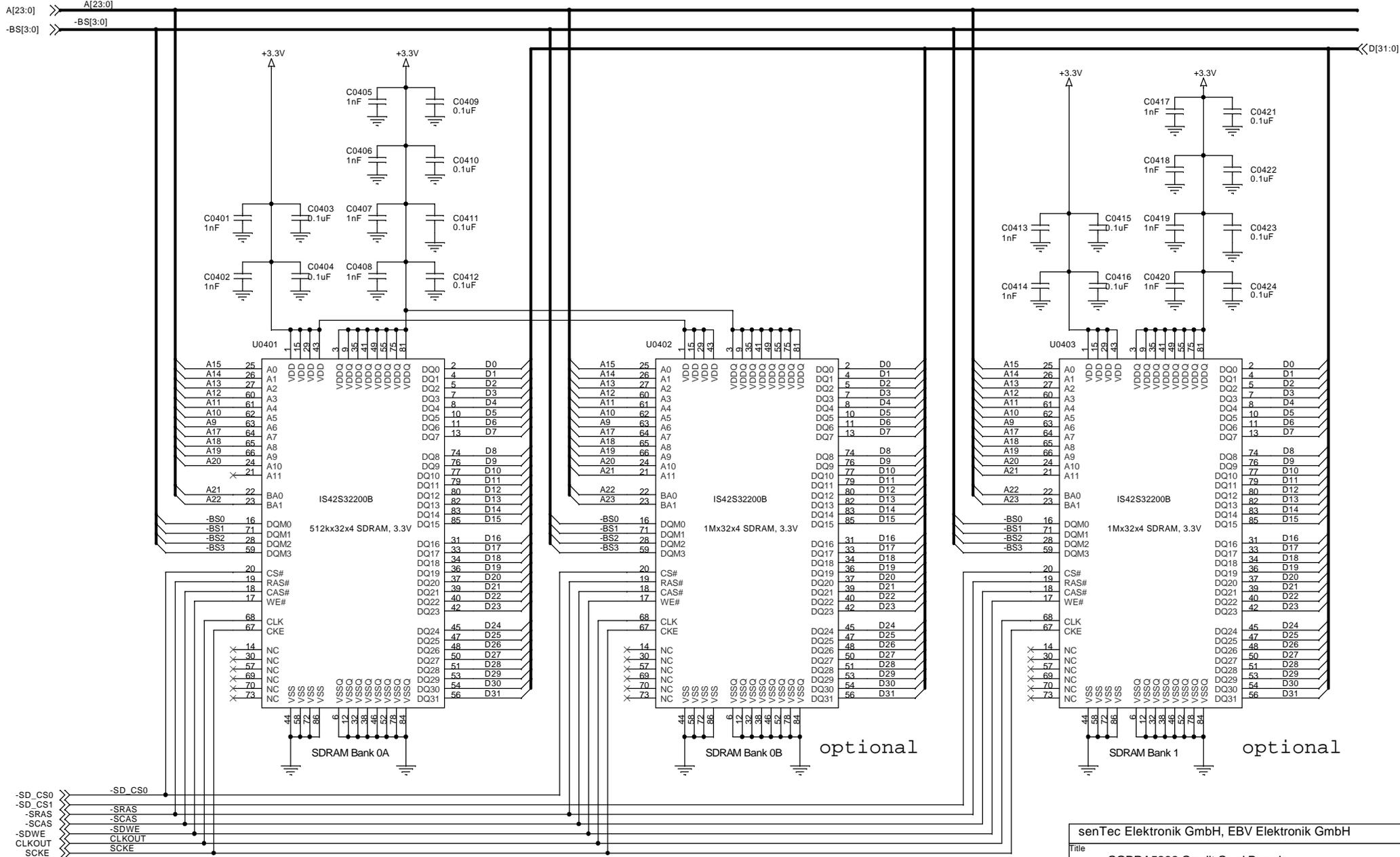
Interrupt 2 can be issued when data is received (wake-up on Ethernet).

Ethernet Configuration 1 1 1:
 Auto-Negotiation Enable
 10BASE-T Half/Full-Duplex
 100BASE-T Half/Full-Duplex
 PHY Address 11111

Ethernet LEDs (Link and Data) should be connected to Vdd.

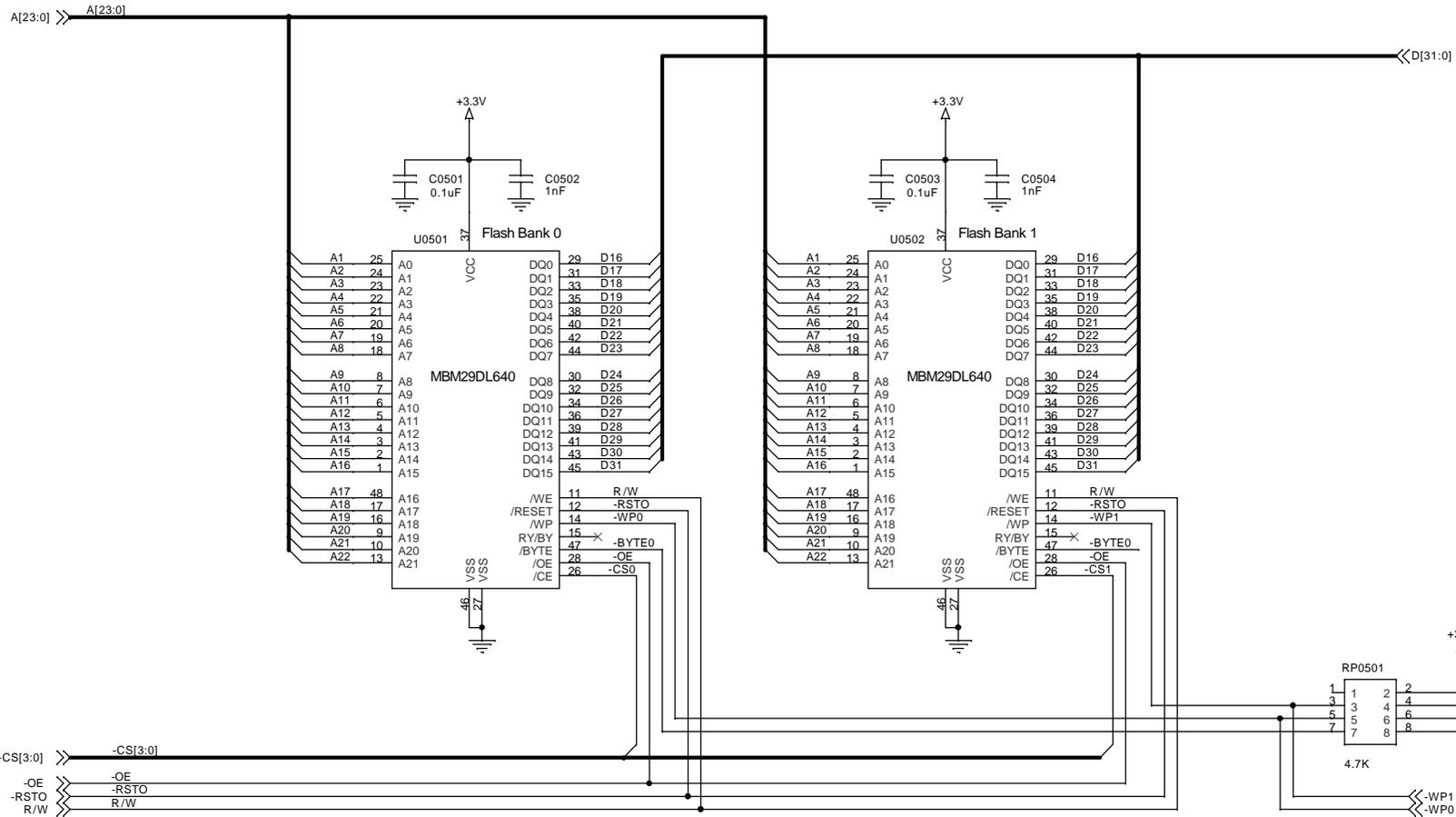
NOTE: Place PHY close to the processor, since in the MII lines are no termination resistors.

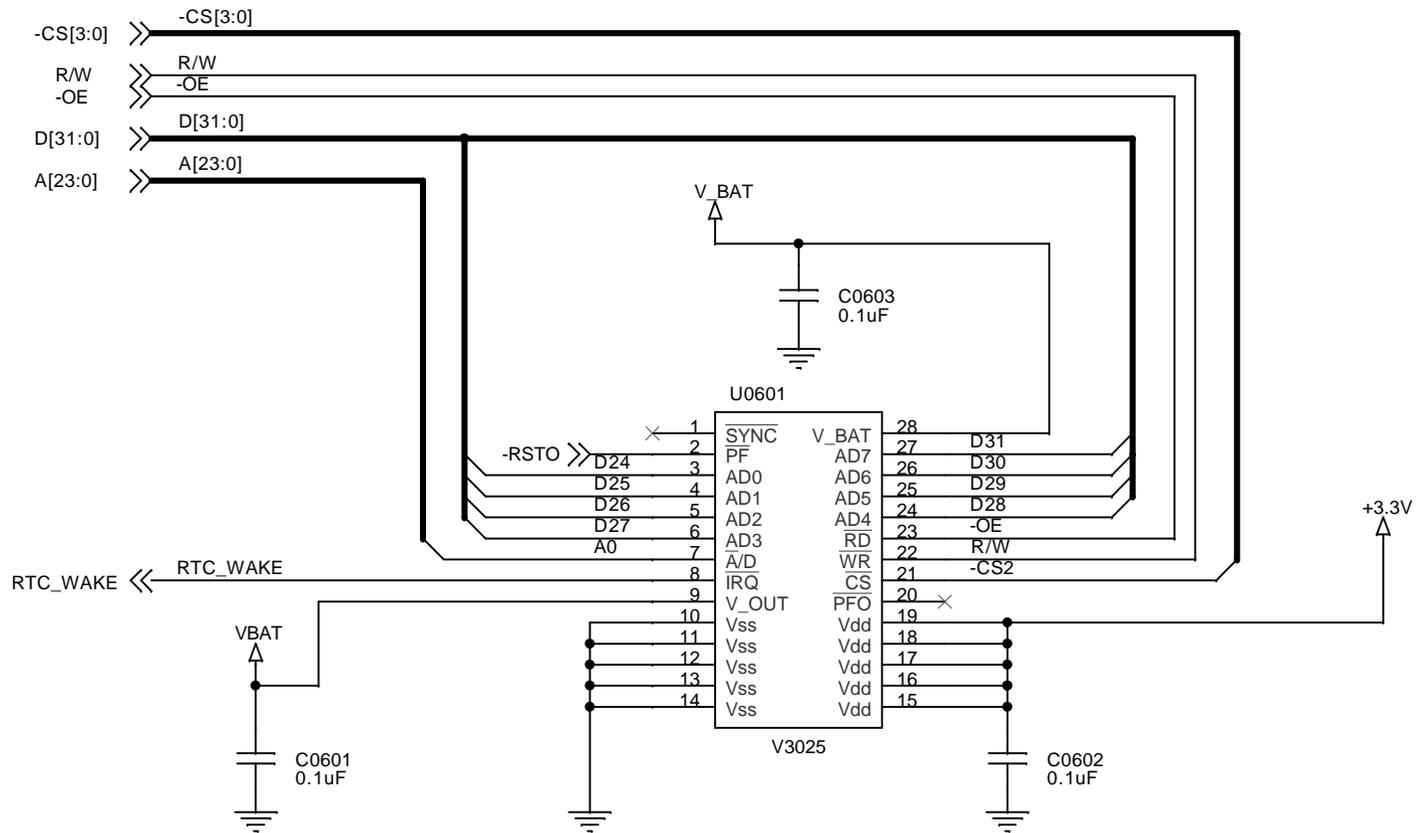
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-SD_CS0
-SD_CS1
-SRAS
-SCAS
-SDWE
CLKOUT
SCKE

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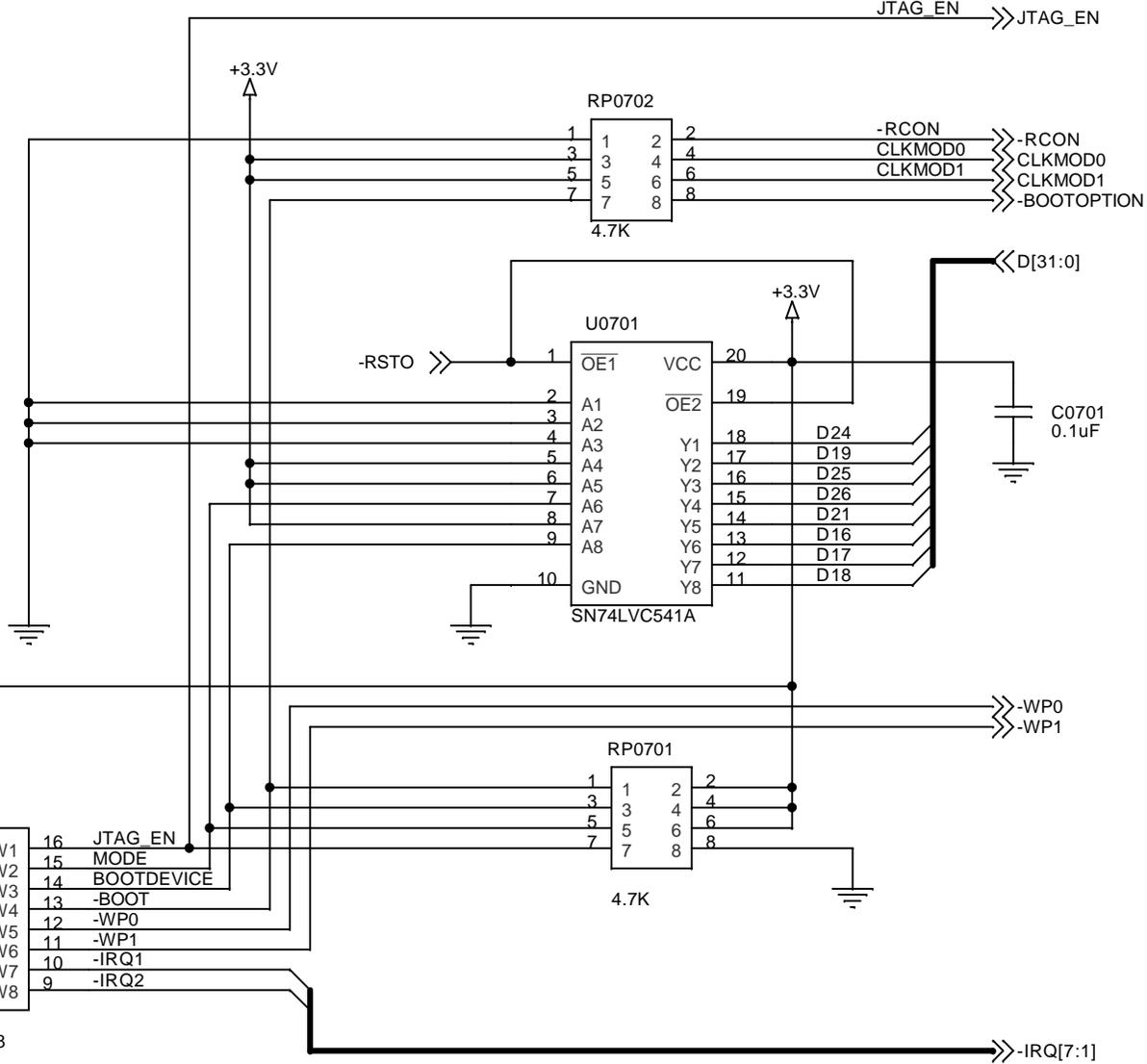
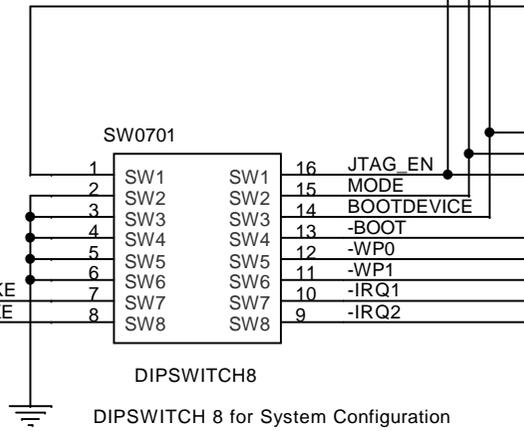




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Chip Configuration:
 -RCON: fixed: L (Chip Configuration ON)
 JTAG_EN: switched: L=BDM; H=JTAG (default = L)
 CLKMOD0: fixed: H (PLL with Crystal)
 CLKMOD1: fixed: H (PLL with Crystal)
 D26: fixed: H
 D17: fixed: H
 D16: switched: H=Master Mode, L=Single Chip Mode (default = H)
 D19: fixed: L
 D18: switched: H=External 16 Bit, L=Internal Boot (default = H)
 D21: fixed: H (full drive, can be reconfigured via software)
 D25: fixed: L (A[23:21])
 D24: fixed: L (A[23:21])

RTC_WAKE
 ETH_WAKE



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