IIM7000A

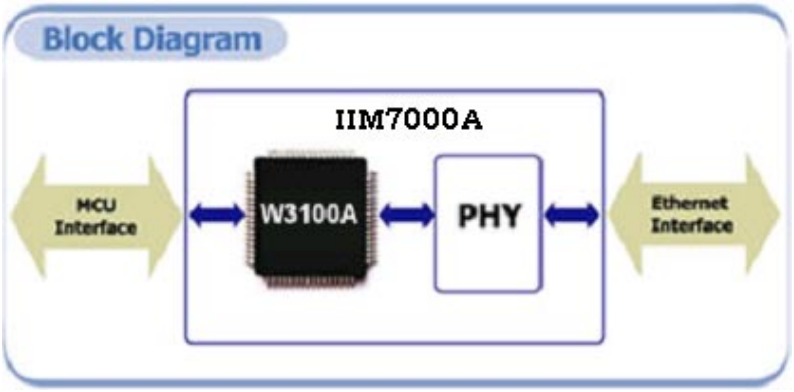
1. Introduction

IIM7000A is the mini network module that includes W3100A (TCP/IP hardwired chip), Ethernet PHY (RTL8201BL) and other glue logics. It can be used as a component and no effort is required to interface W3100A and PHY chip. The IIM7000A is an ideal option for users who want to develop their Internet enabling systems rapidly. Being only 25 mm x 25 mm, IIM7000A operates at 3.3 V (with 5 V-tolerant I/O), has two 24-pin connection headers and auto-detects 10/100 Mbps Ethernet speed.

1.1. Features

- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports Auto-negotiation
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports Intel/Motorola MCU bus Interface
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 12 header pin
- Has compatibility with IIM7000

1.2. Block Diagram



2. Pin Assignments & descriptions

I : Input
O : Output
I/O : Bi-directional Input and output
P : Power

2.1. Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP1 : 1 , JP2 : 24	**Power** : 3.3 V power supply for IIM7000A
GND	P	JP1 : 8, JP1 : 13, JP1 : 24, JP2 : 1 JP2 : 7, JP2 : 13 JP2 : 14, JP2 : 23	**Ground**

2.2. MCU Interfaces

Symbol	Type	Pin No.	Description
A14~A0	I	JP1 : 7, JP1 : 10 JP1 : 9, JP1 : 12 JP1 : 11 JP1 : 14 ~ JP1 : 23	**Address** : 15 bit-wide address bus
D7~D0	I/O	JP2 : 21, JP2 : 22 JP2 : 19, JP2 : 20 JP2 : 17, JP2 : 18 JP2 : 15, JP2 : 16	**Data** : 8 bit-wide data bus
/CS	I	JP1 : 5	**Module Select** : Active low. /CS of W3100A
/RD	I	JP1 : 4	**Read Enable** : Active low. /RD of W3100A
/WR	I	JP1 : 3	**Write Enable** : Active low /WR of W3100A
/INT	O	JP1 : 2	**Interrupt** : Active low After reception or transmission it indicates that the W3100A requires MCU attention. By writing values to the Interrupt Status Register of W3100A the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W3100A(Interrupt Mask Register). For more details refer to the W3100A Datasheet

2.3. Network Interfaces & LEDs

You can observe the network status using MAC-JACK LEDs. LED interface can be extended to the LED of the main board.

Symbol	Type	Pin No.	Description
TPTX+	O	JP2 : 3	**Transmit Output** : Differential pair shared by 100 Base TX and 10 Base Modes. When configured as 100 Base TX,
TPTX-		JP2 : 5	
TPRX+	I	JP2 : 9	**Receive Input** : Differential pair shared by 100 Base TX and 10 Base T Modes.
TPRX-		JP2 : 11	
L_COL	O	JP2 : 6	**Collision LED** : Active low when collisions occur.
L_100ACT	O	JP2 : 8	**Link 100/ACT LED** : Active low when linked by 100 Base TX, and blinking when transmitting or receiving data.
L_10ACT	O	JP2 : 10	**Link 10/ACT LED** : Active low when linked by 10 Base T, and blinking when transmitting or receiving data.
L_LINK	O	JP2 : 12	**Link LED** : Active low when linked

2.4. Reset

Symbol	Type	Pin No.	Description
RESET	I	JP1 : 6	**Reset** : Active high Initializes or Reinitializes the W3100A. Asserting this pin will force a reset process to occur, which will result in all internal registers reinitializing to their default and all strapping options are reinitialized. For complete reset function, this pin must be asserted low for at least 10us.

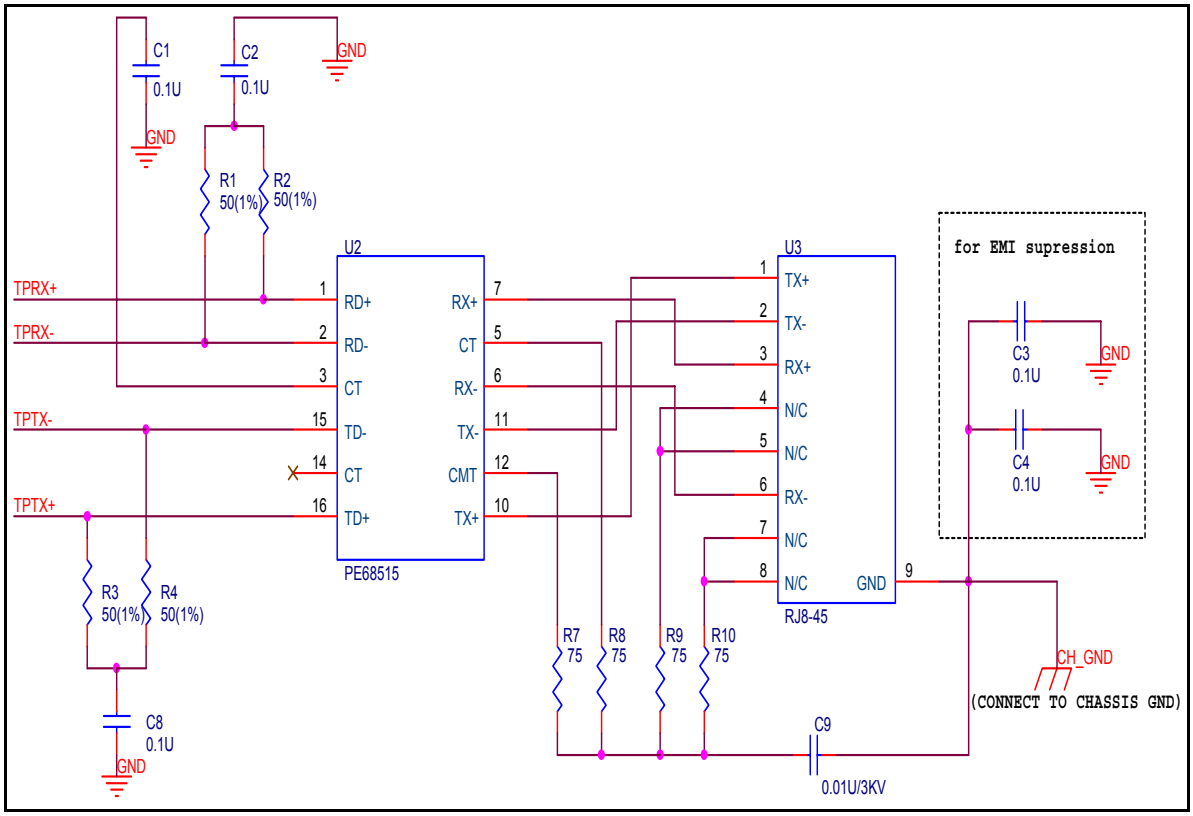
			Refer to W3100A datasheet for further detail regarding reset.
/RESET	I	JP2 : 2	**Reset :** Active low Reset RTL8201BL chip. For complete reset function, this pin must be asserted low for at least 10ms.

3. Transformer Specifications

Parameter	Transmit End	Receive End
Turn Ratio	1 : 1 CT	1 : 1
Inductance (MIN)	350 uH @ 8mA	
Leakage Inductance	0.05 ~ 0.15 uH	
Capacitance (MAX)	15 pF	
DC Resistance (MAX)	0.4 ohm	

Any transformer with Tx/Rx turn ratio of 1:1CT/1:1 is suitable for RTL8201BL, such as Pulse PE68515/H1012, Valor ST6118, YCL 20PMT04, DELTA LF8221, BH16ST8515, TAIMIC HSIP-002.

4. Ethernet Interface (Transformer and RJ45)



5. Timing Diagrams

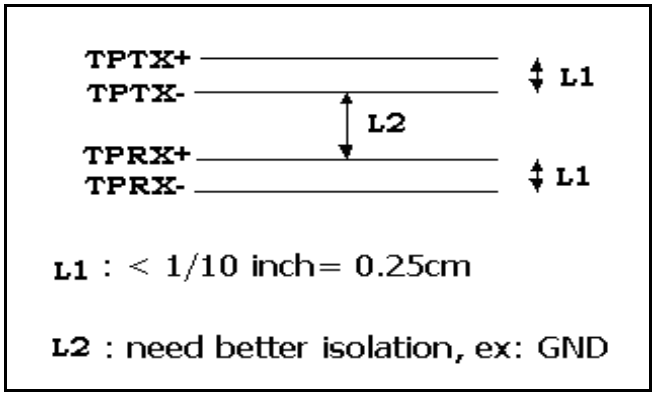
IIM7000A supports only “Clocked Mode”

For more detail information, refer to Datasheet of W3100A.

6. PCB Layout guide

-. TPTX±, TPRX± traces should pay more attention:

- Avoid signal loss on these traces.
- TPTX+, TPTX- should be equal length as possible.
- TPRX+, TPRX- should be equal length as possible.
- The distance between TPTX± and TPRX±:

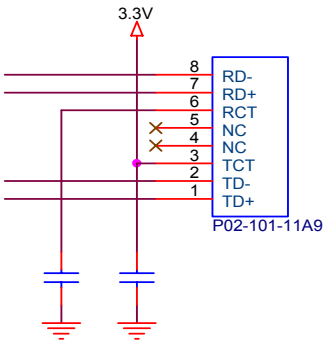
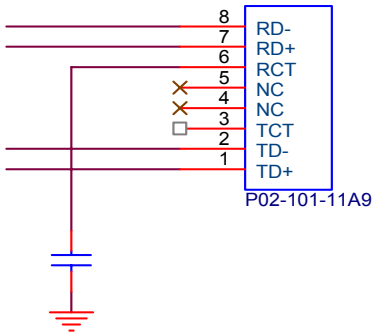


- TPRX± had better not use via.
- Traces routed from RX and TX to the transformer should run in close pairs directly to the transformer. The designer should be careful not to cross the transmit and receive pairs. As always, vias should be avoided as much as possible. The network interface should be void of any signals other than the TX and RX pairs between the RJ-45 to the transformer. There should be no power or ground planes in the area under the network side of the transformer to include the area under the RJ-45 connector.
- For more detail information, refer to "RTL8201BL PCB Layout Guide" document.

7. Design guide for IIM7000 users

Because of the modification of the PHY chip the interface with MAG-JACK is changed. In case of using the RTL8201BL, TCT must be opened as follows

[How to interface with transformer]

1. Transformer schematic for the RTL8201L	2. Transformer schematic for the RTL8201BL
	In case of using the RTL8201BL, TCT must be opened as follows: 

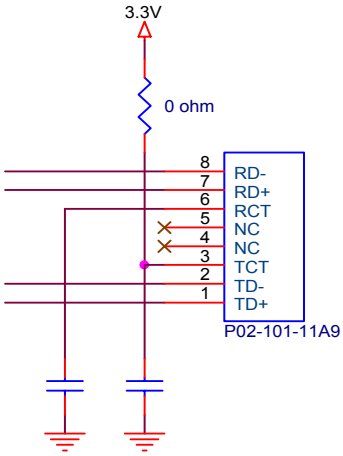
3.RTL8201L, RTL8201BL combined Transformer schematic

In case of RTL8201BL & Transformer

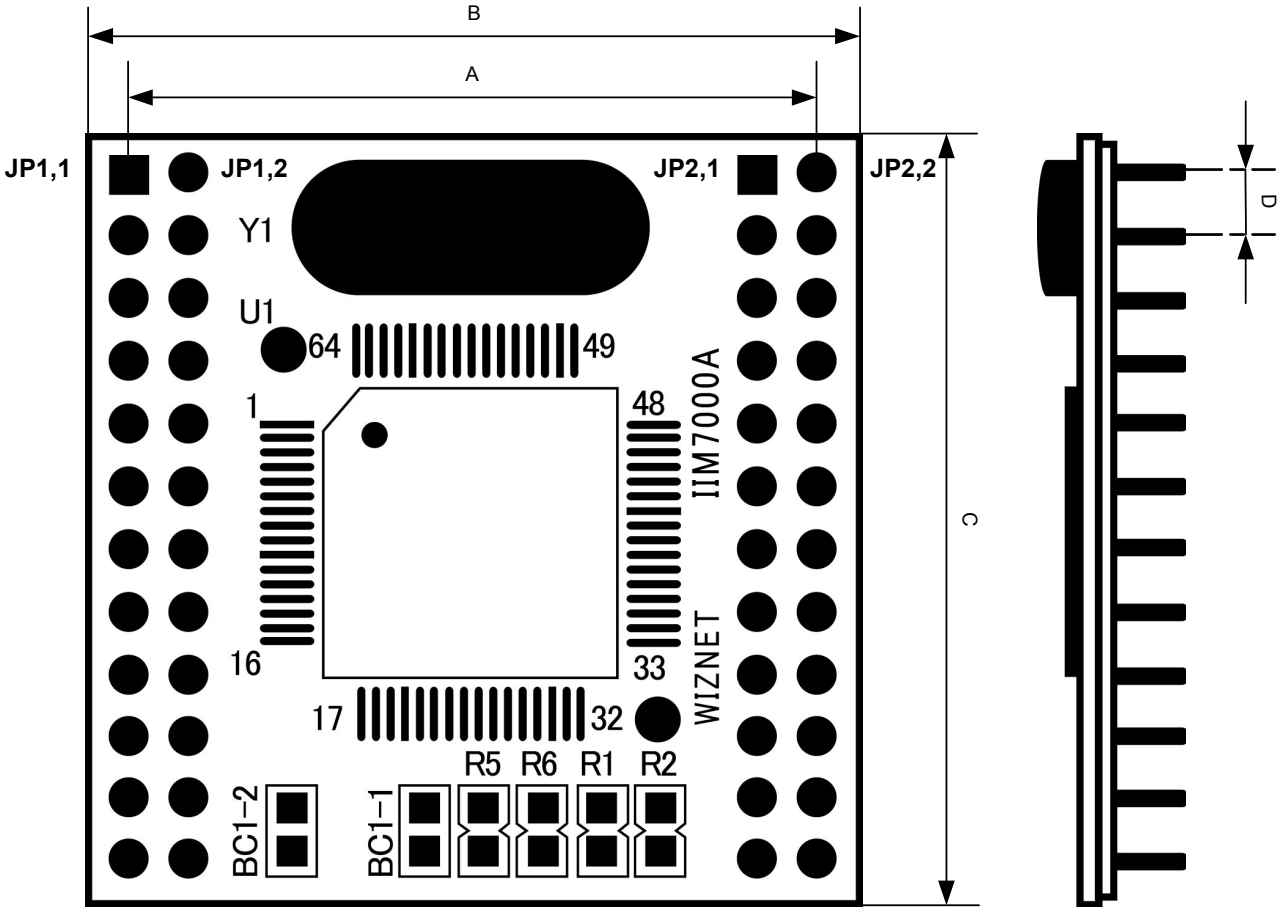
Remove R (Resistor) and C (Capacitor) connected to TCT

In case of RTL8201L & Transformer

Add R (0 Ohm Resistor) or C (Capacitor) to use



8. Dimension



Symbol	Dimension (mm)
A	22.4
B	25.0
C	25.0
D	2.0