Charon II

Ethernut embedded ethernet module

Main Features

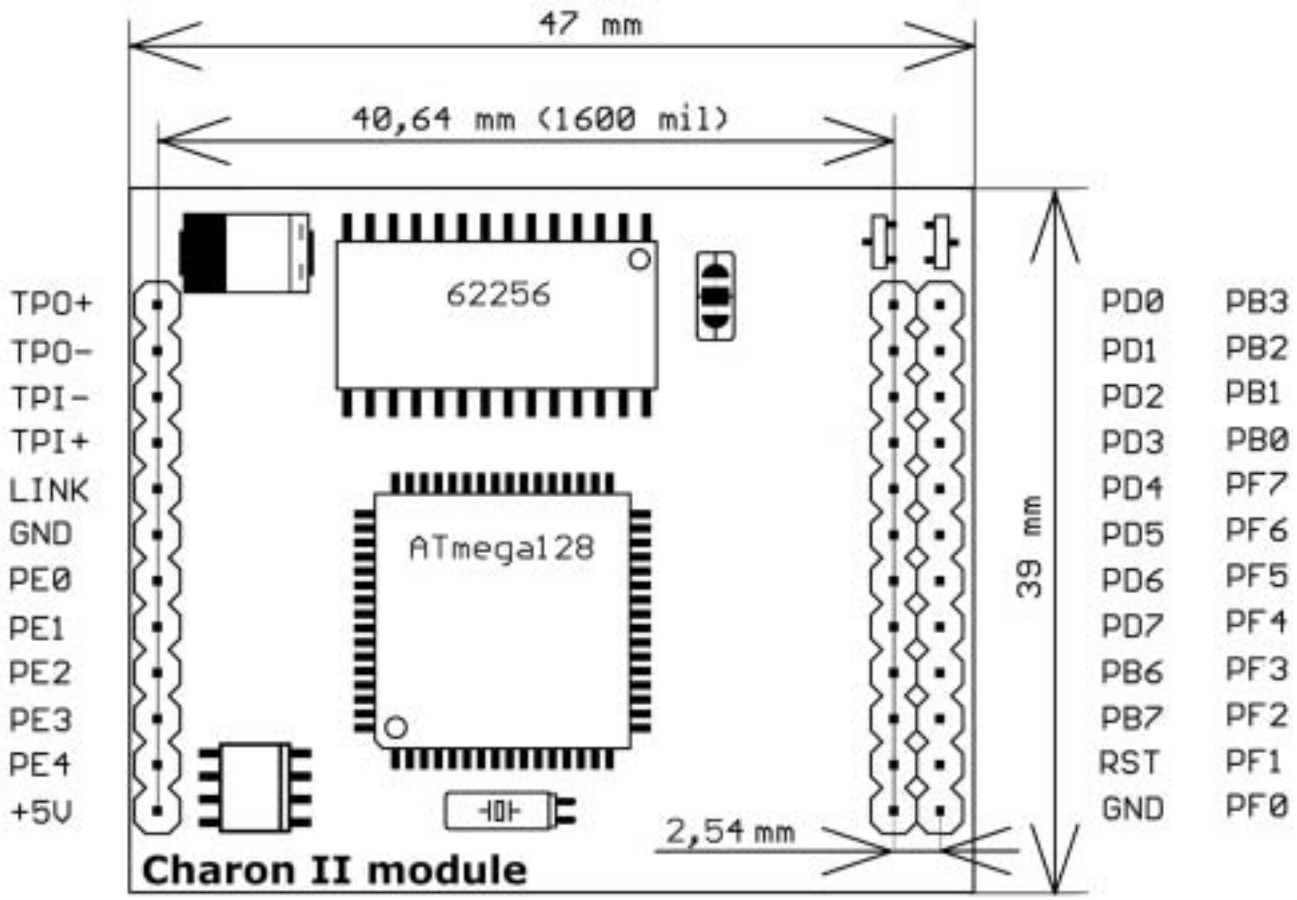
- Full duplex IEEE 802.3 10 Mb/s Ethernet
- ATmega 128 RISC AVR microcontroller - up to 16 MIPS throughput
- 128 kByte In-System Programmable FLASH ROM
- 32 kByte SRAM + 4 kByte internal MCU SRAM
- 4 kByte In-System programmable EEPROM

- Nut/OS - RTOS and TCP/IP stack
  (AVR GCC, ImageCraft ICCAVR, CodeVision AVR)

- Module is SW compatible with Ethernut 1.3 board.
- Development Board and SW examples available.

Interfaces :

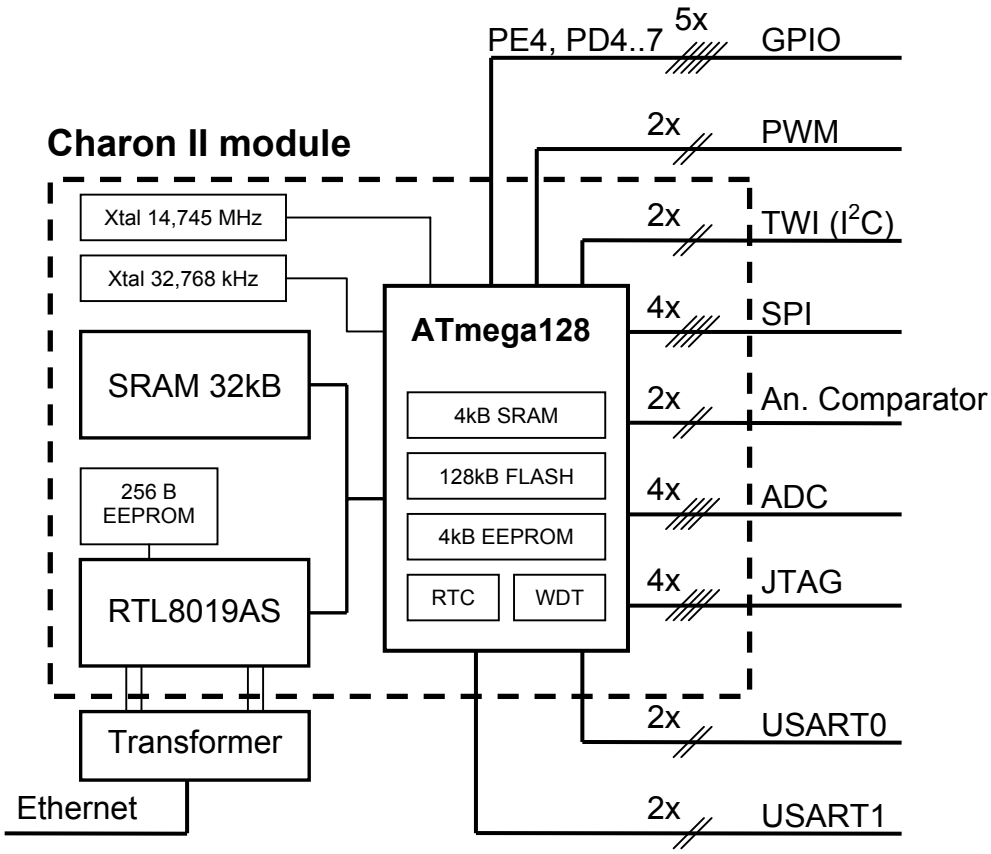
- 2x RS-232 serial ports,
- JTAG interface,
- SPI interface,
- 4x (+ 4x) AD Converter input,
- 2x (+ 4x) PWM output,
- TWI (I^2C) interface,
- 1x Analog Comparator ,
- separated RTC oscillator.



Charon II module - pinout

1	**TPO+**	Ethernet output	INT0/SCL	**PD0**	13	25	**PB3**	SPI MISO
2	**TPO-**	Ethernet output	INT1/SDA	**PD1**	14	26	**PB2**	SPI MOSI
3	**TPI-**	Ethernet input	INT2/RxD1 serial 1	**PD2**	15	27	**PB1**	SPI SCK
4	**TPI+**	Ethernet input	INT3/TxD1 serial 1	**PD3**	16	28	**PB0**	SPI /SS
5	**LINK**	Link LED	IC1	**PD4**	17	29	**PF7**	ADC7/ TDI
6	**GND**	Ground	XCK1	**PD5**	18	30	**PF6**	ADC6/ TD0
7	**PE0**	RxD0 serial 0	T1	**PD6**	19	31	**PF5**	ADC5/ TMS
8	**PE1**	TxD0 serial 0	T2	**PD7**	20	32	**PF4**	ADC4/ TCK
9	**PE2**	AIN+/XCKO	OC1B	**PB6**	21	33	**PF3**	ADC3
10	**PE3**	AIN-/OC3A	OC1C	**PB7**	22	34	**PF2**	ADC2
11	**PE4**	INT4/OC3B	MCU reset pin	**RST**	23	35	**PF1**	ADC1
12	**Vcc**	+5V /max 80 mA	Ground	**GND**	24	36	**PF0**	ADC0

Charon II block scheme:



Hardware Description

Parameters	
Power supply	*5V DC / typ. 60mA max 80 mA*
Dimension	*47 x 39 x 12 mm (L x W x H)*
Temperature	*Operating: -5 .. +50 °C*
Ethernet	*10BaseT – 802.3 (external signal transformer required)*
2xSerial port	*TTL levels RxD,TxD*
Programming	*SPI In-System Programming* *JTAG interface (std. IEEE 1149.1)*

Charon II – standard version	
MCU Xtal	*14.745 MHz*
SRAM / EEPROM	*4+28 kB /(4kB MCU internal)*
RTL8019 EEPROM	*256B (93C46) – optional*
27 I/O pins	*GPIO (7), ADC(4), JTAG (4)* *2x RS-232 (4), SPI(4), I²C(2)*
Power-on reset	*YES – 10% tolerance*
WATCHDOG	*MCU internal WD only*
Real Time Clock	*Separated timer 32.768 kHz*

- Charon II module is compatible with the original **Ethernut board 1.3F** from the Ethernut project (www.Ethernut.de).
- It's a low cost embedded alternative without the HW accessible Address bus (it's accessible on the original board).
- You can start designing with this module using **Charon II Development Kit**.
  It includes a simple programmer dongle SW compatible with AVR Studio and STK500, 2x16 LCD display, 1-Wire Thermometer sensor, Printed manual and a well-documented functional example on using all peripherals.

Module pin description

(1) TPO+, (2) TPO-, (3) TPI+, (4) TPI-,

10Base -T Differential outputs and inputs. You have to connect this to the signal transformer. See the "**Connecting to the Ethernet**" chapter for more details, or "**Charon II module application circuit**" on the Appendix.

(5) LINK - Link LED output to Vcc

Link activity signalization output. It's lit when an Ethernet burst signal is detected on the Ethernet input and the LED is pulsed during outgoing or incoming packets over Ethernet.

(6) GND - Ground

Internally connected with ground on pin 24.

(7) PE0 - RxD0 serial 0 [PDI/RXD0 (Programming Data Input or UART0 Receive Pin)]

PDI, SPI Serial Programming Data Input: During Serial Program Downloading, this pin is used as data input line for the ATmega128.

RXD0, USART0 Receive Pin: Receive Data (Data input pin for the USART0). When the USART0 receiver is enabled this pin is configured as an input regardless of the value of DDRE0. When the USART0 forces this pin to be an input, a logical one in PORTE0 will turn on the internal pull-up.

(8) PE1 - TxD0 serial 0 [PDO/TXD0 – Port E, Bit 1]

PDO, SPI Serial Programming Data Output: During Serial Program Downloading, this pin is used as data output line for the ATmega128.

TXD0, UART0 Transmit pin.

(9) PE2 - AIN+/XCKO [AIN0/XCK0 – Port E, Bit 2] CTS handshake input for serial 0

AIN0 (AIN+) – Analog Comparator Positive input: This pin is directly connected to the positive input of the Analog Comparator.

XCK0, USART0 External clock: The Data Direction Register (DDE2) controls whether the clock is output (DDE2 set) or input (DDE2 cleared). The XCK0 pin is active only when the USART0 operates in Synchronous mode.

(10) PE3 - AIN-/OC3A [AIN1/OC3A – Port E, Bit 3] RTS handshake output for serial 0

AIN1 (AIN-) – Analog Comparator Negative input: This pin is directly connected to the negative input of the Analog Comparator.

OC3A, Output Compare Match A output: The PE3 pin can serve as an External output for the Timer/Counter3 Output Compare A. The pin has to be configured as an output (DDE3 set "one") to serve this function. The OC3A pin is also the output pin for the PWM mode timer function.

(11) PE4 - INT4/OC3B [Port E, Bit 4]

INT4, External Interrupt source 4: The PE4 pin can serve as an External Interrupt source.

OC3B, Output Compare Match B output: The PE4 pin can serve as an External output for the Timer/Counter3 Output Compare B. The pin has to be configured as an output (DDE4 set (one)) to serve this function. The OC3B pin is also the output pin for the PWM mode timer function.

SJ1 on board jumper is placed on the module (check the Charon II module scheme). If you need battery backup for the external SRAM only, you can cut off the PE4 pin from the MCU and using SJ1, SRAM is powered through this pin only.

(12) Vcc +5V / max. 80 mA

Module only power consumption in the "Charon II Development Board". It's measured using the Demo application, no sleep mode or power saving mode used.

– during active RESET I = **40 mA**
– PING reply only I = **60 mA**
– during WEB activity I = **65 mA**

(13) PD0 - INT0/SCL [External Interrupt 0 Input or TWI (I^2C) Serial CLock]

INT0, External Interrupt source 0: The PD0 pin can serve as an external interrupt source to the MCU.

SCL, Two-wire Serial Interface Clock: When the TWEN bit in TWCR is set (one) to enable the Two-wire Serial Interface, pin PD0 is disconnected from the port and becomes the Serial Clock I/O pin for the Two-wire Serial Interface. In this mode, there is a spike filter on the pin to suppress spikes shorter than 50 ns on the input signal, and the pin is driven by an open drain driver with slew-rate limitation.

(14) PD1 - INT1/SDA [External Interrupt1 Input or TWI (I^2C) Serial DAta]

INT1, External Interrupt source 1: The PD1 pin can serve as an external interrupt source to the MCU.

SDA, Two-wire Serial Interface Data: When the TWEN bit in TWCR is set (one) to enable the Two-wire Serial Interface, pin PD1 is disconnected from the port and becomes the Serial Data I/O pin for the Two-wire Serial Interface. In this mode, there is a spike filter on the pin to suppress spikes shorter than 50 ns on the input signal, and the pin is driven by an open drain driver with slew-rate limitation.

(15) PD2 - INT2/RxD1 serial 1 [External Interrupt2 Input or UART1 Receive Pin]

INT2, External Interrupt source 2: The PD2 pin can serve as an External Interrupt source to the MCU.

RXD1, Receive Data (Data input pin for the USART1): When the USART1 receiver is enabled this pin is configured as an input regardless of the value of DDD2. When the USART forces this pin to be an input, the pull-up can still be controlled by the PORTD2 bit.

(16) PD3 - INT3/TxD1 serial 1 [External Interrupt3 Input or UART1 Transmit Pin]

INT3, External Interrupt source 3: This pin can serve as external interrupt source to the MCU.

TXD1, Transmit Data (Data output pin for the USART1): When the USART1 Transmitter is enabled, this pin is configured as an output regardless of the value of DDD3.

(17) PD4 - IC1 [IC1 (Timer/Counter1 Input Capture Trigger)]

IC1 – Input Capture Pin1: The PD4 pin can act as an input capture pin for Timer/Counter1.

(18) PD5 - XCK1 [XCK1, USART1 External Clock Input/Output]

XCK1, USART1 External clock: The Data Direction Register (DDD4) controls whether the clock is output (DDD4 set) or input (DDD4 cleared). The XCK1 pin is active only when the USART1 operates in Synchronous mode.

(19) PD6 - T1 [Timer/Counter1 Clock Input]

T1, Timer/Counter1 counter source.

(20) PD7 - T2 [Timer/Counter2 Clock Input]

T2, Timer/Counter2 counter source.

(21) PB6 - OC1B [Output Compare and PWM Output B for Timer/Counter1]

OC1B, Output Compare Match B output: The PB6 pin can serve as an external output for the Timer/Counter1 Output Compare B. The pin has to be configured as an output (DDB6 set (one)) to serve this function. The OC1B pin is also the output pin for the PWM mode timer function.

(22)PB7 - OC2/OC1C [Output Compare and PWM Output for Timer/Counter2 or Output Compare and PWM Output C for Timer/Counter1]

OC2, Output Compare Match output: The PB7 pin can serve as an external output for the Timer/Counter2 Output Compare. The pin has to be configured as an output (DDB7 set “one”) to serve this function. The OC2 pin is also the output pin for the PWM mode timer function.

OC1C, Output Compare Match C output: The PB7 pin can serve as an external output for the Timer/Counter1 Output Compare C. The pin has to be configured as an output (DDB7 set (one)) to serve this function. The OC1C pin is also the output pin for the PWM mode timer function.

(23) RST - CPU reset pin [MCU External Reset input] **L = MCU in Reset**

An External Reset for the MCU is generated by a low level on the RST pin. Reset pulses longer than the minimum pulse width (50ns) will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

During the supply power-up the module is **reset** with an external and internal voltage supervisor.

The **RST pin** on the module is **bidirectional**. It can reset external circuitry upon a reset caused by MCU software or the voltage supervisor, connected through the R6 - 3k3 resistor.

(24) GND - Ground

Internally connected with ground on pin 6.

(25) PB3 - SPI MISO [SPI Bus Master Input/Slave Output]

MISO: Master Data input, Slave Data output pin for SPI channel. When the SPI is enabled as a master, this pin is configured as an input regardless of the setting of DDB3. When the SPI is enabled as a slave, the data direction of this pin is controlled by DDB3. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB3 bit.

(26) PB2 - SPI MOSI [SPI Bus Master Output/Slave Input]

MOSI: SPI Master Data output, Slave Data input for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB2.
When the SPI is enabled as a master, the data direction of this pin is controlled by DDB2.
When the pin is forced to be an input, the pull-up can still be controlled by the PORTB2 bit.

(27) PB1 - SPI SCK [SPI Bus Serial Clock]

SCK: Master Clock output, Slave Clock input pin for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB1.
When the SPI is enabled as a master, the data direction of this pin is controlled by DDB1.
When the pin is forced to be an input, the pull-up can still be controlled by the PORTB1 bit.

(28) PB0 - SPI /SS [SPI Slave Select input]

SS: Slave Port Select input. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB0. As a slave, the SPI is activated when this pin is driven low. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB0.
When the pin is forced to be an input, the pull-up can still be controlled by the PORTB0 bit.

(29) PF7 - ADC7/ TDI [ADC input channel 7 or JTAG Test Data Input]

ADC7: Analog to Digital Converter, Channel 7.

TDI, JTAG Test Data In: Serial input data to be shifted in to the Instruction Register or Data Register (scan chains). When the JTAG interface is enabled, this pin can not be used as an I/O pin.

(30) PF6 - ADC6/ TD0 [ADC input channel 6 or JTAG Test Data Output]

ADC6: Analog to Digital Converter, Channel 6.

TDO, JTAG Test Data Out: Serial output data from Instruction Register or Data Register. When the JTAG interface is enabled, this pin can not be used as an I/O pin.

The TDO pin is tri-stated unless TAP states that shift out data are entered.

(31) PF5 - ADC5/ TMS [ADC input channel 5 or JTAG Test Mode Select]

ADC5: Analog to Digital Converter, Channel 5.

TMS, JTAG Test Mode Select: This pin is used for navigating through the TAP-controller state machine. When the JTAG interface is enabled, this pin can not be used as an I/O pin.

(32) PF4 - ADC4/ TCK [ADC input channel 4 or JTAG Test ClocK]

ADC4: Analog to Digital Converter, Channel 4.

TCK, JTAG Test Clock: JTAG operation is synchronous to TCK. When the JTAG interface is enabled, this pin can not be used as an I/O pin.

(33) PF3 - ADC3 [ADC input channel 3]

Analog to Digital Converter, Channel 3

(34) PF2 - ADC2 [ADC input channel 2]

Analog to Digital Converter, Channel 2

(35) PF1 - ADC1 [ADC input channel 1]

Analog to Digital Converter, Channel 1

(36) PF0 - ADC0 [ADC input channel 0]

Analog to Digital Converter, Channel 0

Other ATmega pins

PE5 - INTernal on module used only

INT5, External Interrupt source 5: The PE5 is used as an Interrupt request from the RTL8019AS Ethernet controller.

Module programming

In-System Programming (ISP)

Charon II module can be programmed using an **In-System Programming** interface. This programming requires the following pins:

- **ISP MOSI** – **Pin (7) PE0 RxD0 serial 0** (Alternated with USART 0 serial data input)
- **ISP MISO** – **Pin (8) PE1 TxD0 serial 0** (Alternated with USART 0 serial data output)
- **ISP SCK** – **Pin (27) PB1** (Alternated with SPI SCK (SPI Bus Serial Clock))
- **RST** – **Pin (23) RST** MPU reset pin
- **GND** – **Pins (6,24)** Ground
- **+5V** – **Pin (12)** Power supply

This programming mode requires special hardware called a programming adapter, also called a programming **dongle**. Just three pins are used in this mode, an input line, an output line and a clock line. In addition, the RESET line of the chip must be held low during programming. Because serial programming is done while the chip is already soldered onto the target board, it is also called In-System Programming**.**
On the ATmega128 the ISP input and output lines are shared with the transmit and receive lines of the first on-chip USART. This adds a minor problem. As long as the adapter is connected, the output line of the adapter shares the same MCU input line as the RS-232 receiver output, which is included on almost any ATmega128 board. To overcome this, Atmel used an additional line called programming enable or programming LED. The programming software on the PC will set this line low before starting the programming cycle. This line can be used to switch the pins on the ATmega from the RS-232 driver to the ISP connector.

On Ethernut version 1.3 or Charon I&II Development Board this is done by a multiplexer chip and the line will also light the red programming LED. But not all programming adapters provide this signal, so there is a jumper on the Charon II Development Board (15 – ISP LED & STK500 programming jumper) or the Ethernut 1.3 board. With this jumper the signal can manually pull the line low = enable ISP programming.

HW STK 500 dongle – ISP Programmer

HW STK500 dongle contained in the **Charon II Development Kit** is a copy of the original **SISP** from the original Ethernut Project. There are some non-compatibility issues with the original STK500 adapter. We are working on this, but it's only a tool for Charon II module programming.

For more details about this, please check Ethernut project article:
ISP Adapter (**http://www.ethernut.de/en/isp/)**

JTAG Programming

JTAG is completely different from ISP. It can not only program the target device, but adds additional hardware and software debugging support. And it requires a more advanced programming adapter which costs much more than a simple ISP adapter.
Atmel's "low cost" JTAG adapter, called **AT JTAGICE**, comes with an adapter cable, it can be used directly with the **Charon I&II Development Board**.

Due to the high price of JTAG adaptors compared to ISP adapters, JTAG adapters are mainly used for application debugging.

MCU Programming with using Network Loader

There are several methods to upload your software to a target device like an Ethernut Board or Charon II module is. One of the most advanced is using an Ethernet bootloader (http://www.ethernut.de/en/eboot/) based on the DHCP, BOOTP and TFTP protocols.

Default ATmega128 MCU Fuses & Lock bits settings

All modules are tested and shipped with following Lock bits setting. The ATmega128 MCU has three fuse bytes, this listing of the Charon II default settings is organised under AVR Studio - STK500 - Fuses tab.

Note that the fuses are read as logical zero : "**1**" means **un-programmed**
"**0**" means **programmed**
"**X**" means **any value**

Fuse	Value	Description
M103C	1	ATmega103 compatibility mode
WDTON	1	Watchdog Timer always on
OCDEN	1	Enable OCD
***JTAGEN**	0	Enable JTAG *(PF4 – PF7 use for JTAG only)*
SPIEN	0	Enable Serial Program and Data Downloading
EESAVE	1	EEPROM memory is preserved through the Chip Erase
BOOTSZ1	X	Select Boot Size
BOOTSZ0	X	Select Boot Size
BOOTRST	1	Select Reset Vector
BODLEVEL	1	Brown out detector trigger level *(BODLEVEL=2.7V)*
BODEN	0	Brown out detector enable
CKOPT	0	Oscillator options *(Ext. Crystal/Resonator High Freq.)*
SUT1	1	Select start-up time
SUT0	1	Select start-up time *(Start-up time + 64 ms)*
CKSEL3	1	Select Clock source
CKSEL2	1	Select Clock source
CKSEL1	1	Select Clock source
CKSEL0	1	Select Clock source *(Start-up time = 16K CK)*

**** JTAG pins** – The **PB0, PB1, PB2, PB3** pins are used for JTAG programming, because of this, you can't use it free while the JTAG interface is enabled (default state).*

Lock Bits

LB mode	LB2	LB1	Protection Type
1	1	1	No memory lock features enabled.

Application Protection Mode

BLB0 mode	BLB02	BLB01	Protection Type
1	1	1	No restrictions for SPM or (E)LPM accessing the Boot Loader section.

Boot Loader protection

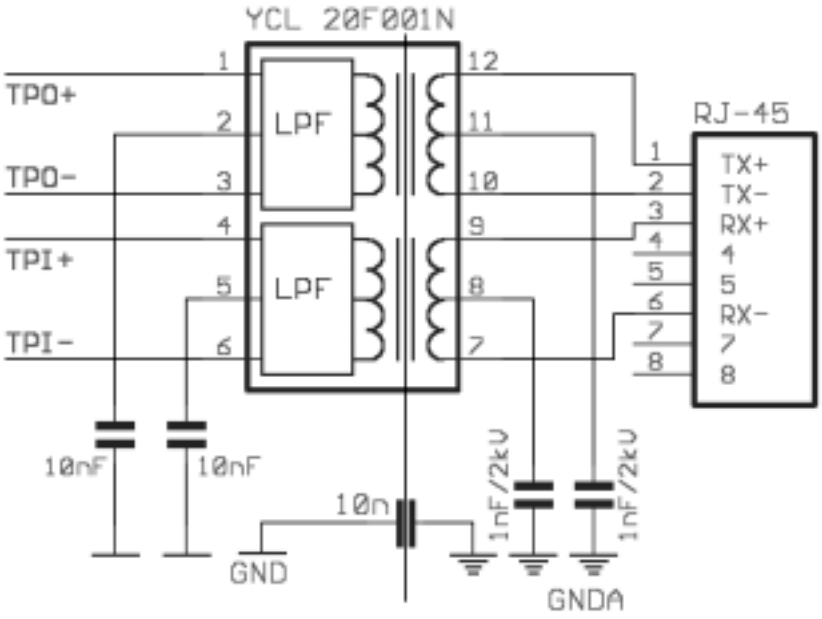
BLB1 mode	BLB12	BLB11	Protection Type
1	1	1	No restrictions for SPM or (E)LPM accessing the Application section.

Connecting to Ethernet

There is no placed Ethernet transformer, on the module. You have to place it to your application board. It's a simple scheme and you can order this transformer from us with the module. We recommend connecting the Ethernet outputs according to the following recommended diagram. You can choose separated transformer as "DIL14" size component (YCL 20F001N or Bothhand FS2022). If you need save PCB space, you can use transformer together with the RJ45 connector in one component (LF1S022).

IN EVERY CASE, PLEASE PAY ATTENTION TO THE SEPARATION OF THE ETHERNET AND APPLICATION GROUNDS! - It can cause very strange troubles.

YCL 20F001N – Transformer + RJ 45 connector



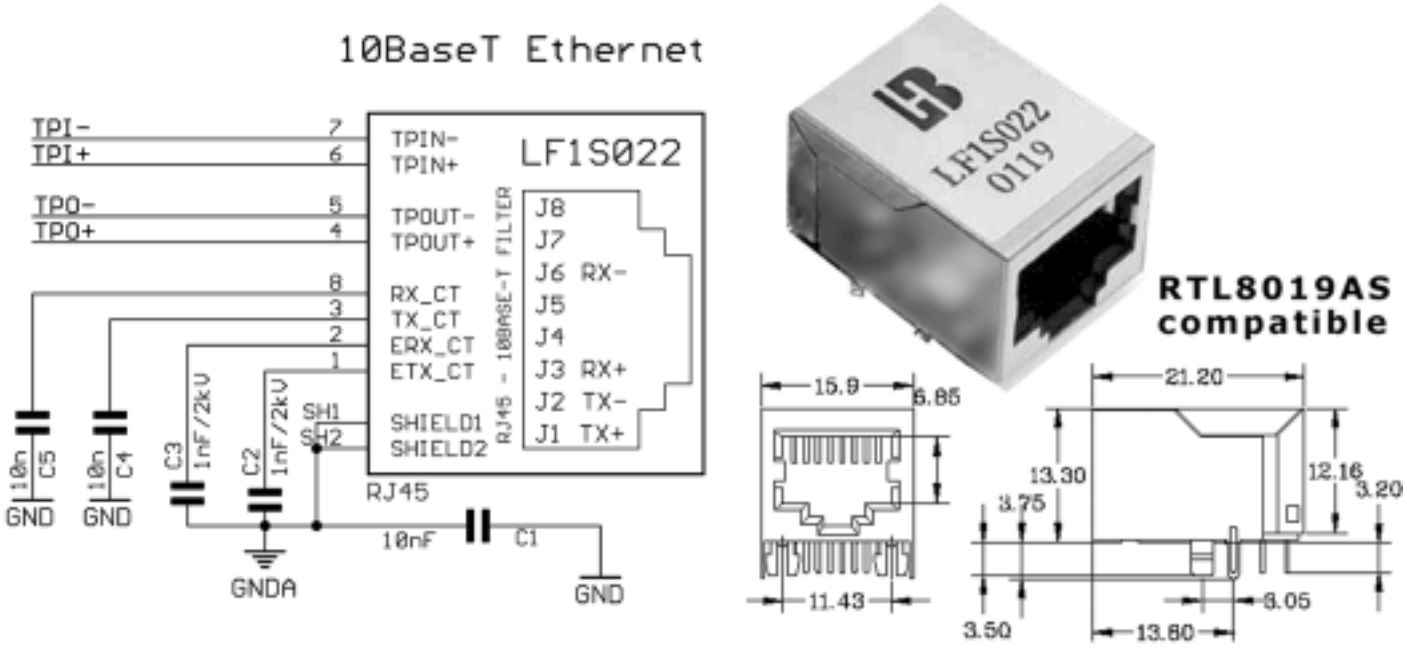
Separated transformer is a little better suited for industrial applications due to increased insulation strength, thanks to the standard packaging of the magnetic.

You can find some transformer datasheets on the CD to the Charon II Development Kit.

You can see separated GND and GNDA on this scheme.

The termination resistor 100Ω on the TPI pair, known from the Charon I module is already placed on the Charon II module.

LF1S022 – Transformer integrated with the RJ45 connector



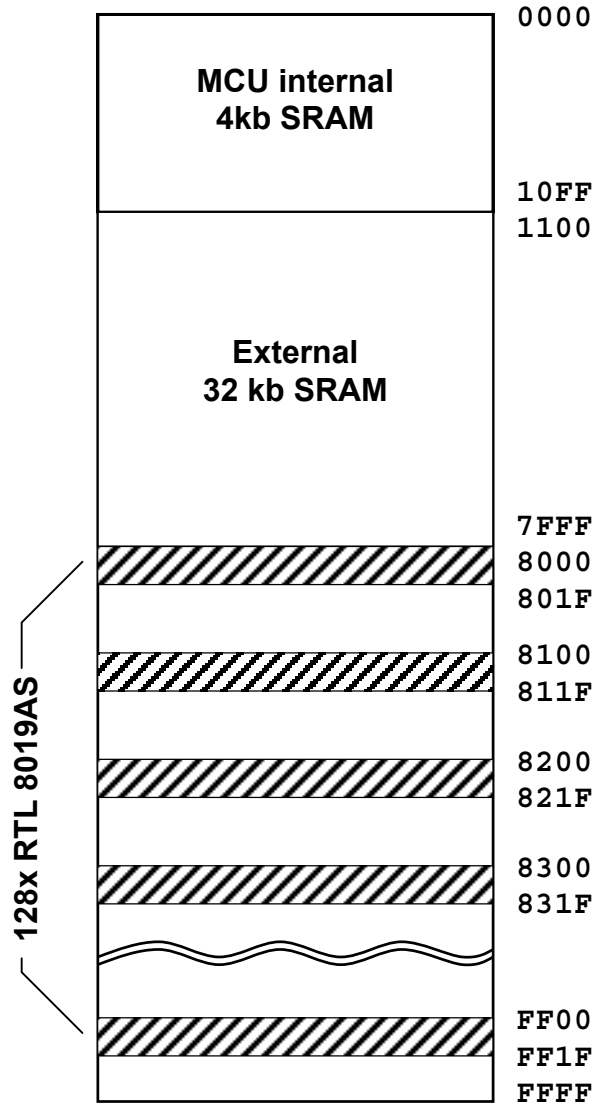
Address space – Ethernut ver. 1.3F compared to Charon II

Internal and external RAM address spaces are wired identically on the Ethernut 1.3F board and Charon II module. But the ethernet controller driver Realtek 8019AS is mapped in the I/O devices address space (0x8000 – 0xFFFE) many times (8000h, 8100h, 8200h, 8300h, …. FE00h, FF00h), according to original Ethernut 1.3F board where the RTL8019AS is mapped on the on 8300h-831F address only and space 8320h-FFFF is free to other I/O devices.

ATmega128 MCU SRAM space

- 0x0000 – 0x10FF …internal Atmega128 CPU RAM space
- 0x1100 – 0x7FFF …external 32 kB SRAM address space
- 0x8000 – 0xFFFF…I/O devices address space

On the Charon II module it isn't possible to map devices to the address space (address and data bus isn't available on the connectors), finally it's 100% SW compatible with the original Ethernut board software.



Related & Development tools

Charon II Development Kit

The Charon II module is available in the Development Kit with the programmer, application board, SW examples and others:

- The **Charon II** module with MAC address and serial number on the label.
- The **Charon I&II Development Board** (Shortly Development Board only).

- An **HW STK-500** compatible programming adapter for serial RS-232 port.
- A **LapLink serial communication cable** with a DB-9 female socket on both ends.
- The **DS1822** 1-Wire thermometer sensor
- A **LCD display 2x16**
- **CD** with all necessary software in the **/Charon2/** directory
- Printed **Module** and **Development Kit** datasheets.

Development Kit contains full documented example on using all peripherals contained on Development Board (Digital Inputs/Outputs, 1-Wire thermometer, Serial port, LCD display, ..) using a simple WWW demo page.

Check the Charon II Development Kit manual

Hyperion box

This is HW group's baseboard & metal enclosure for the Charon II module. If you are interested we can send you board scheme and the enclosures mechanical dimension for use in your designs.

The following peripherals are used on the base board:

- 9..15V linear power supply
  or 6..35V switched power supply
- Backup Battery 3.6 V
- 1x full RS-232 serial port (75176 driver]
- 1x RS-232 / 485 serial port
- SPI serial FLASH
- 10 Mbit Ethernet with using RJ45
- 4x DIP switch
- 4x screw terminal strip (RS-485 + power)

Contact us for more details..

Recommended literature

- www.Ethernut.de
  Original site for the Ethernut project with all source code in actual version
- **Charon II Development Kit**
  Getting Started guide + example description (www.HW-group.com)
- **Charon II Development Board**
  Scheme of our DK board shows how to connect peripherals to the Charon II module.

- www.HW-group.com
  Authors of the Charon II module and related products..
- **ATmega128, RTL8019AS Datasheets**
  All Datasheets for used components included on Development Kit CD.

Acknowledgement

We want to thank to Mr. H. Kipp from the Egnite company – authors of the Ethernut project for his big work on this project, opening project to other developers and their support…

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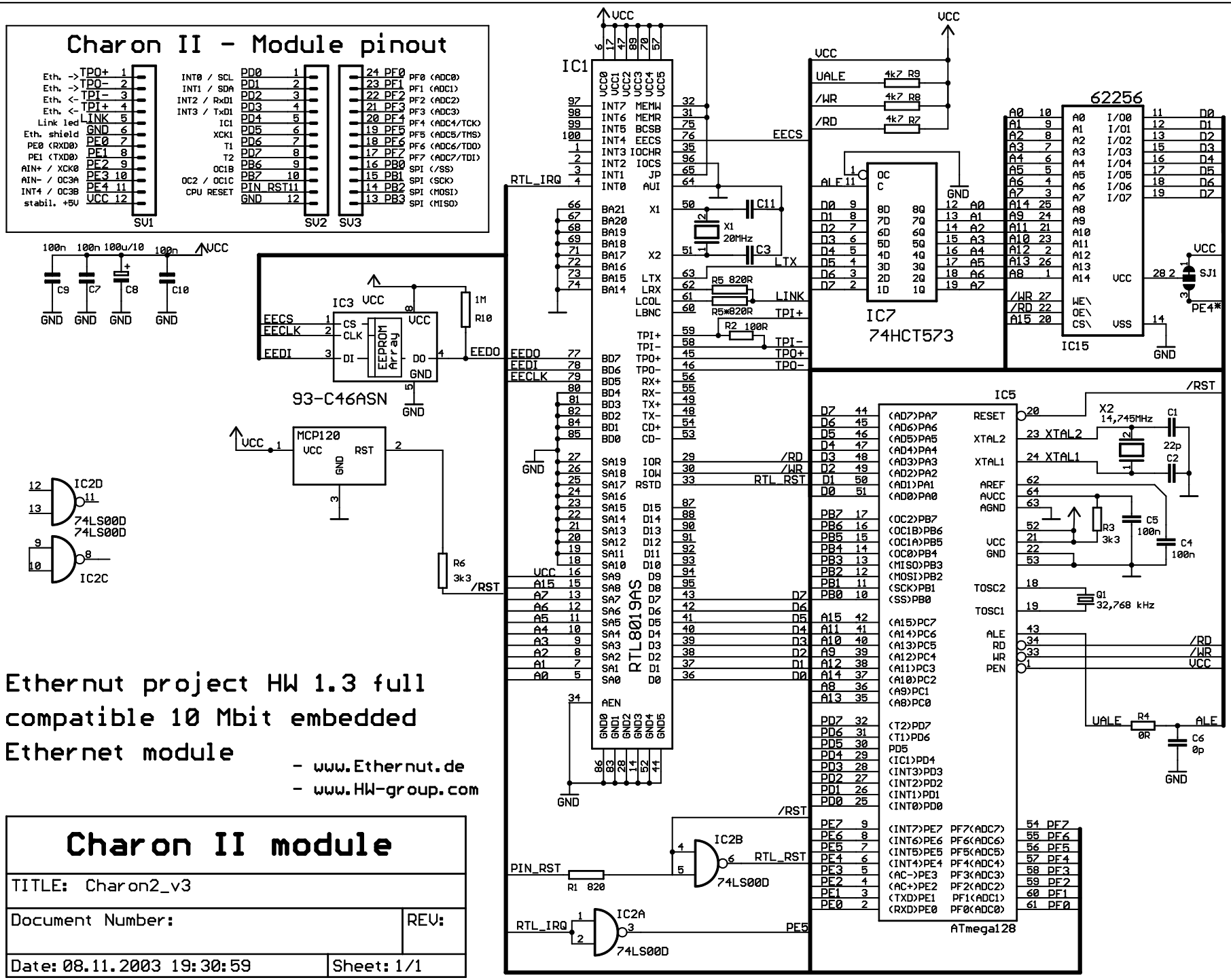
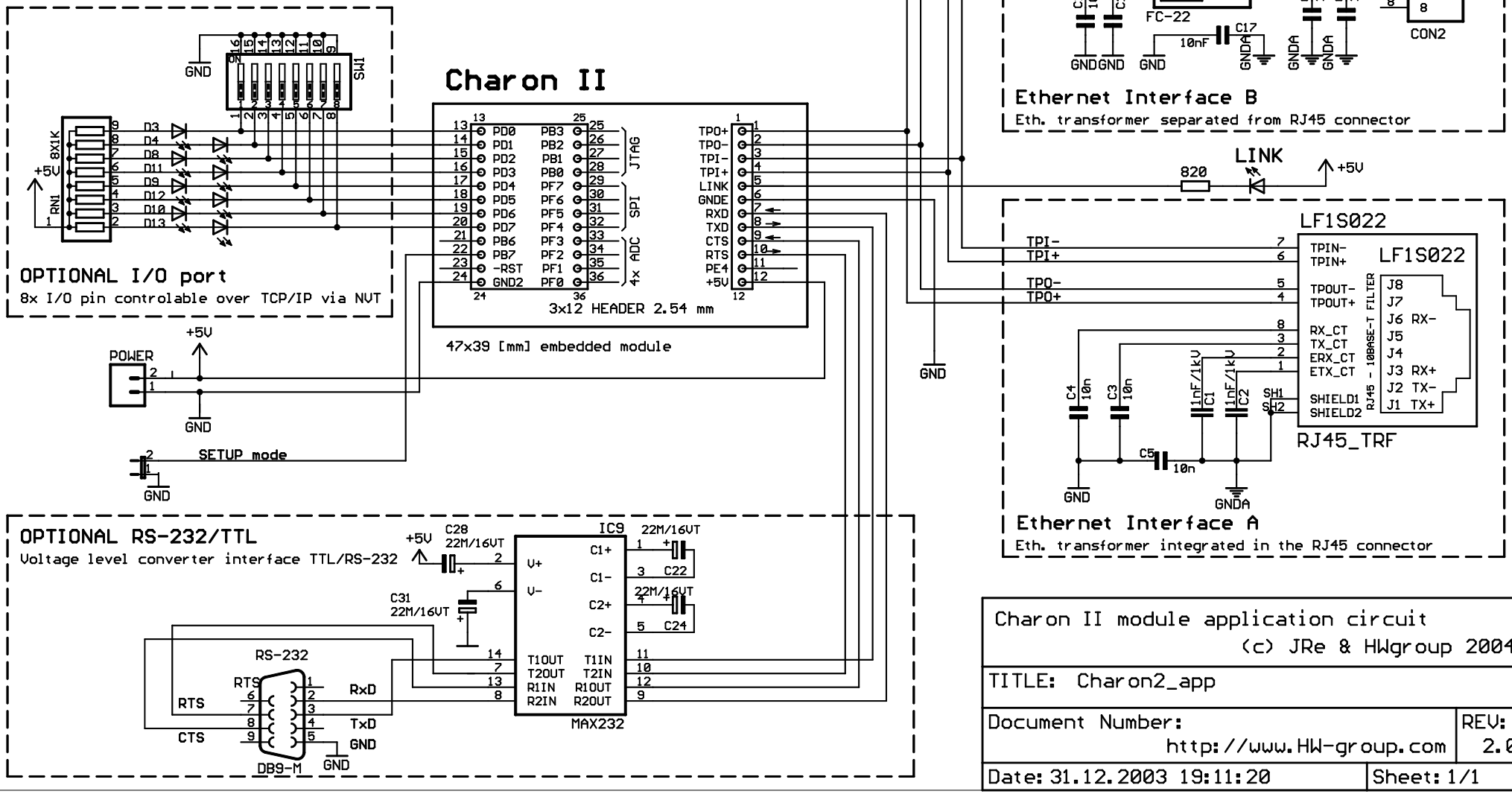

Charon II - Module pinout
SV1
SV2
SV3
IC1
RTL8019AS
IC3
93-C46ASN
IC7
74HCT573
62256
IC15
IC5
ATmega128
X1
20MHz
X2
14,745MHz
Q1
32,768 kHz
MCP120
IC2A
IC2B
IC2C
74LS00D
Ethernut project HW 1.3 full compatible 10 Mbit embedded Ethernet module
- www.Ethernut.de
- www.HW-group.com
Charon II module
TITLE: Charon2_v3
Document Number:
REV:
Date: 08.11.2003 19:30:59
Sheet: 1/1

MANDATORY PINS: Vcc(+5V), GND,RxD,TxD,
TPO+,TPO-,TPI-,TPI+

Ethernet interface: select one type (A or B)
A - LF1S022 + 5x capacitor only
B - YCL20F001N + RJ45 connector

Keep SEPARATED device's GND from the Ethernet's GNDA!

Check the "Charon II Development Board" scheme for reccomended connection of various external peripherals to the Charon II module.



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